

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Initially, it is noted that Applicants filed a claim for priority under 35 U.S.C. § 119(a)-(d) and a certified copy of German Patent Application 102 44 664.4, filed September 24, 2002, in the instant application on September 24, 2003. However, in items 12, 12a and 12a1 of the Office Action Summary the Examiner has not confirmed receipt of Applicants' claim for priority and certified copy. The Examiner's confirmation of receipt of such papers would be appreciated.

It is also noted that Applicants filed an invention disclosure, a certified English translation of the same and a Declaration under 37 CFR 1.131 on August 24, 2005 to overcome the Saeki reference, U.S. Patent No. 6,717,252. That reference should therefore have been overcome. However, in the Response to Arguments, the Examiner has stated that "the affidavit filed 8/24/05 was not processed by the office to determine its accuracy." This statement is not understood. If there is some processing to be done by the Office, Applicants request that it be done. Since the Examiner has not questioned the evidence shown in the declaration, it is believed that the Saeki reference should not have been cited in item 5 of the above-identified Office action.

Claims 1-21 remain in the application. Claims 13-21 are subject to examination and claims 1-12 have been withdrawn from examination. Claims 1 and 13 have been amended. No claims have been added or canceled.

Once again rejoinder of method claims 1-12 is requested and is required by MPEP 821.04. The amendments made to claim 13 herein have also been made to claim 1.

In "Claim Rejections - 35 USC § 102", item 2 on pages 2-4 of the Office Action, claims 13-14, 16-17 and 20-21 have been rejected as being fully anticipated by U.S. Patent No. 6,353,263 to Dotta et al. (hereinafter Dotta) under 35 U.S.C. § 102(e).

In "Claim Rejections - 35 USC § 103", item 4 on page 5 of the Office Action, claim 15 has been rejected as being obvious over Dotta in view of U.S. Patent No. 6,392,304 to Butler under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103", item 5 on pages 5-6 of the Office Action, claims 18 and 19 have been rejected as being obvious over U.S. Patent No. 6,717,252 to Saeki in view of U.S. Patent Application Publication No. US 2002/0130404 to

Ushijima et al. (hereinafter Ushijima) under 35 U.S.C. § 103(a). As mentioned above, the previously filed declaration has removed Saeki as a reference and therefore claims 18 and 19 are assumed to be allowable. In addition, the Examiner mentions "Saeki as applied to claims 13-14 above." However, Saeki is not used in the rejection of claims 13-14. Therefore, it appears that for this reason as well, the application of Saeki against the claims of the instant application is an error.

The rejection of claim 13 has been noted and claim 13 has been amended in an effort to even more clearly define the invention of the instant application.

Support for the changes in claim 13 regarding the intermediate substrate and the rewiring structure being disposed on an active surface of the semiconductor chip, is found on page 3, lines 15-18 and page 12, lines 15-22 of the Specification of the instant application. A typographical error at the end of claim 13 has also been corrected.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 13 calls for, *inter alia*, an electronic component, comprising:

a rewiring substrate having a central area with connecting pads for forming flipchip connections, said rewiring substrate having edge areas with connecting pads;

at least one first lower electronic module formed by a semiconductor chip, said lower electronic module having contact areas electrically connected using flipchip technology to said connecting pads in said central area of said rewiring substrate, said lower electronic module having a passive rear face;

at least one second upper electronic module including a semiconductor chip with an active surface and a rewiring structure with an intermediate substrate and external contact surfaces, said rewiring structure being disposed on said active surface of said semiconductor chip, said upper electronic module having a passive rear face resting against said passive rear face of said lower electronic module;

a plurality of bonding connections between said external contact surfaces of said upper electronic module and said connecting pads in said edge areas of said rewiring substrate; and

a component package surrounding said upper electronic module and said lower electronic module.

The Dotta reference discloses a semiconductor device and manufacturing method therefor. Fig. 1 of Dotta discloses a first chip 1 and a second chip 2 having a bonding agent 7 therebetween. The chips are disposed on a substrate 3 having external terminals 10 and are covered by a resin coat 9. Since the chip 2 is larger than the chip 1, it is supported by a support structure 21 of conductive bonding agent 20.

Dotta does not disclose a second upper electronic module which includes a rewiring structure with an intermediate

substrate and external contact surfaces as recited in amended claim 13.

The electronic component according to the amended independent claim 13 is, therefore, not anticipated by Dotta under 35 USC 102.

The electronic component according to amended claim 13 is also not obvious over the prior art, as will be explained below.

Dotta fails to teach an upper electronic module including a the wiring structure with an intermediate substrate and external contact surfaces, which is disposed on the active surface of the semiconductor chip.

The provision of a rewiring structure with an intermediate substrate and external contact surfaces according to the invention has the advantage of providing a more reliable electronic component, since the upper electronic module has the necessary robustness for handling in a test procedure. This advantage of the claimed structure is described in detail from page 3, line 15 to page 9, line 17 of the Specification of the instant application.

Dotta teaches that the reliability of the electronic component is improved by providing the support portion 21 formed by protruding portions of the bonding agent 20 which covers flip chip contacts of a lower semiconductor chip. This support portion 21 supports the protruding regions of the larger upper semiconductor chip 2 so as to enable the wire bonds to be reliably formed between the upper semiconductor chip 2 and the rewiring substrate 3 of the semiconductor device.

Dotta provides no motivation for one skilled in the art to seek a further modification by which the reliability of a semiconductor device could be improved, and no motivation for the person skilled in the art to seek a further modification by which the reliability of the wire bonds is improved. That is because Dotta teaches that this is successfully achieved by use of support portions of the bonding agent. Since Dotta teaches the advantages of the support regions 21, Dotta gives a skilled artisan no incentive to modify by omitting the support regions 21.

Even if the skilled person did decide to improve the semiconductor device of Dotta, Dotta provides the skilled person with no reason to do this by providing a rewiring structure with an intermediate substrate and external contact

surfaces positioned on the active surface of the upper electronic module.

Furthermore, none of the other cited prior art documents teach a semiconductor device in which the upper electronic module includes a rewiring structure with an intermediate substrate and external contact areas. The other cited prior art documents also fail to teach a rewiring structure on an upper electronic module which is surrounded by a component package.

It is, therefore, not obvious from the prior art that a configuration of a rewiring structure with an intermediate substrate and external contact surfaces on the active surface of the semiconductor chip of the upper electronic module has any technical advantage or that such a configuration could improve the reliability of the electronic component. The skilled person, therefore, has been given no incentive to provide an electronic component with the features according to amended claim 13 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 13. Claim 13 is, therefore, believed to be patentable over the art. The

dependent claims are believed to be patentable as well because they all are ultimately dependent on independent claim 13.

In view of the foregoing, reconsideration and allowance of claims 13-21 and the issuance of a Notice of Allowance for claims 1-21, are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner Greenberg Sterner LLP, No. 12-1099.

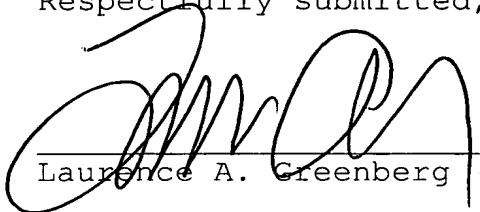
Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Sterner LLP, No. 12-1099.

It is also noted that a new Information Disclosure Statement is enclosed, mentioning references cited in a Search Report dated December 20, 2005 from the European Patent Office for

Appl. No. 10/669,539
Amdt. dated 2/6/06
Reply to Office action of November 4, 2005

the counterpart European application.

Respectfully submitted,



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